Design and Simulation of an X Band LC VCO

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***Abstract*- In this paper, a systematic method for the design of circuit parameters of a monolithic LC Voltage Controlled Oscillator (VCO) is reported. The method is based on the negative resistance generation technique. As a result, a VCO has been designed in 0.18um CMOS technology using a conventional VCO structure to obtain the optimum values for the phase noise and power consumption. The simulation results prove that the proposed approach is very reliable and can be developed further for more complex structures. In this paper, the minimum phase noise of -110.94 dBc/Hz has been obtained at 1 MHz offset frequency at the operating frequency of 10.67 GHz. Furthermore, the designed VCO has the low power consumption of 1.8 mW at the fundamental frequency. In addition, the designed VCO has 1280 MHz of tuning range from 9.39 GHz to 10.67 GHz around the central frequency of 10 GHz. Other than that, the maximum output power of the signal in the designed VCO is 6.24 dBm.**

***Index Terms*-** LC VCO. CMOS. Phase Noise. Design Method. Monolithic.

I. INTRODUCTION

VCO has different functions in any telecommunication system. For instance, it is used in transmitters and receivers as a Local Oscillator (LO), or in Phase Locked Loop (PLL) for clock recovery. Besides, VCOs are widely used in frequency synthesizers [1]. In the design of RF circuits, especially in the VCO, phase noise is a critical parameter due to its effect on the output performance of the oscillator [2]. In the recent telecommunication systems, there is a high demand for robust VCO performance. Therefore, several attempts have been made to optimize the VCO phase noise [3-6]. Another important parameter which should be taken into account in the design of VCOs is its power consumption. This is due to this fact that the low power consumption is the main requirement for the wireless telecommunication systems [7]. Generally, there are two fundamental techniques for

Manuscript received 17-June-2018 and revised 25-Sept.-2018,
Accepted on 10- Nov.-2018
P- ISSN: 2322-4088
E- ISSN: 2322-3936

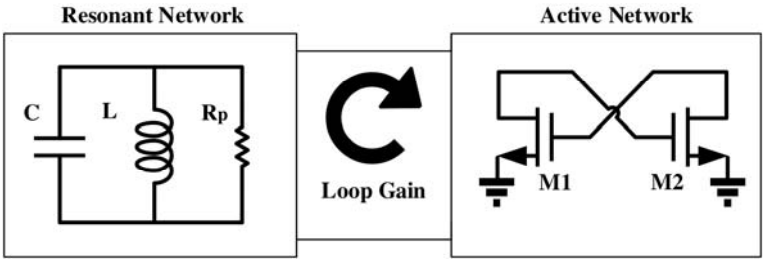


Fig. 1. Negative resistance concept in designing monolithic VCOs.

designing VCO which are negative resistance and feedback amplifier [8]. The majority of the proposed monolithic VCOs are based on the negative resistance technique and the main contributions are related to changing the VCO structure [9-11].

Fig. 1 shows a negative resistance type VCO. As can be seen in Fig. 1, in this type of VCO there must be one active network to compensate the loss in the LC resonator and maintain the oscillation. The remainder of this paper ia organized as follows. Section 2 proposes a systematic fundamental approach for designing a VCO core. Then, the improvement to the structure can be made to optimize the core design and boost up the VCO performance. In section 3, we have designed a Class-B VCO using the proposed approach. In order to simulate this work, we have used KeySight ADS version 2016.01 which the output simulated results show that the proposed VCO is more efficient as compared to that of the state-of-the-art designs. Finally, main results are summarized in section 4.

II. THEORETICAL MODELING

Although several researchers have contributed to the development of the VCOs, there have been very few efforts to propose a detailed and fully explained design method for high performance VCOs. In addition, there are few papers which clearly describe the design procedure for a VCO. In this paper, we propose a design method which can boost up the LC VCO performance in terms of power consumption and phase noise. The following algorithm is a design procedure which is proposed for the design of a high performance LC VCO. In the first steps of the proposed algorithm as shown in Fig. 2, it is required to set some predefined values as expected power consumption or expected output frequency in order to calculate the required values for the components on the VCO core. The proposed design method can be easily extended to different VCO structures due to the fundamental electronic rules used in the algorithm. In order to have a high performance and small size VCO using the conventional Class-B VCO structure shown in Fig. 3, inductance, capacitance and size of the transistors need to be calculated. Based on our proposed algorithm, after setting the predefined values of the power consumption and expected operating frequency of the VCO, the required biasing current should be calculated by simply dividing required power consumption to the supply voltage. The existing biasing current source should generate high impedance between inductors and supply voltage

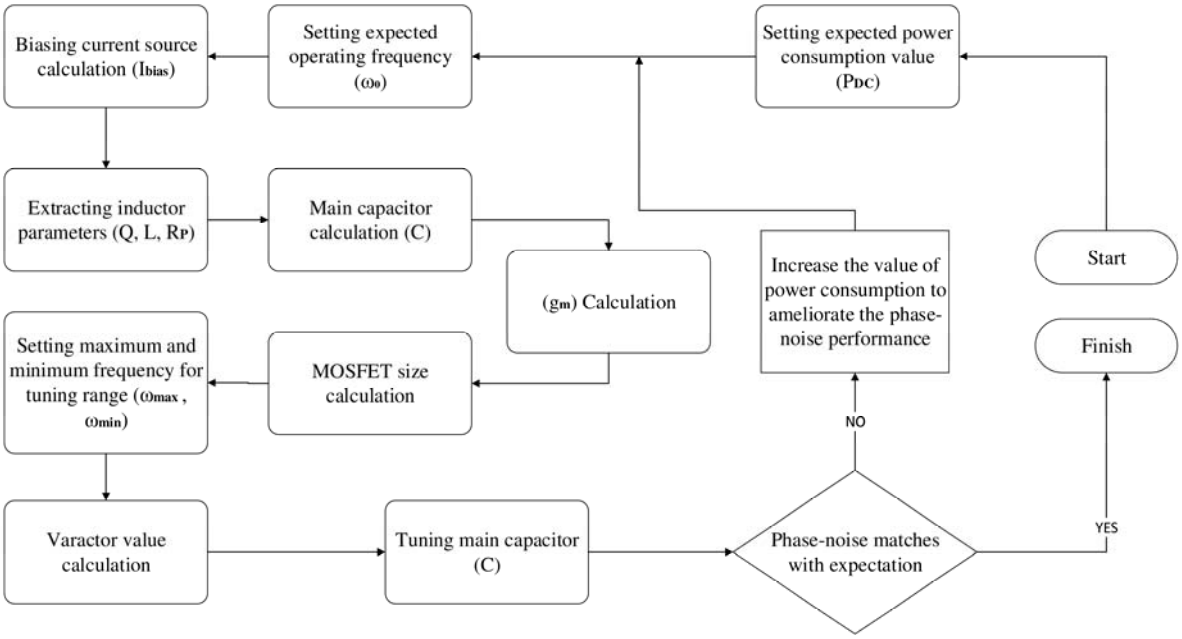


Fig. 2. The proposed algorithm to design a high performance VCO.

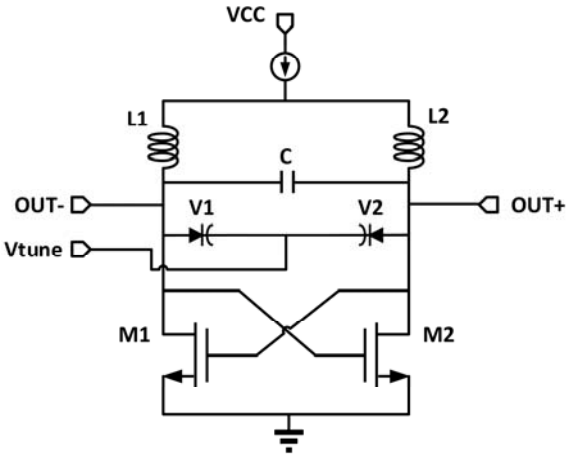


Fig. 3. Conventional VCO core circuit.

to prevent the leaked RF energy from resonator into the supply voltage and keep the output waveform clean and smooth. Fig. 4 shows the difference between the output waveform of the VCO with and without the current source.

Moreover, the mentioned current source will bias the VCO circuit including M1 and M2 transistors. The advantage of our proposed design is its adaptability for different CMOS technologies such as 0.18 um, 0.13 um, 90 nm etc. which each of them endure particular supply voltage for turning on and biasing.

The biasing current (I_{bias}) can be calculated as follow:

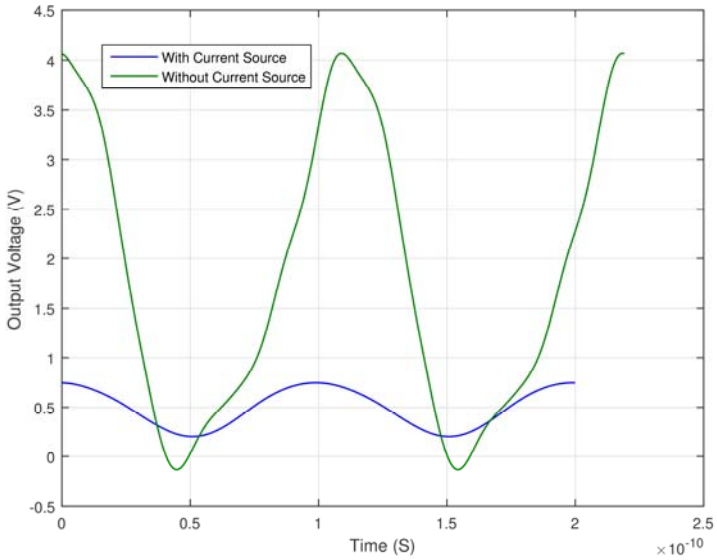


Fig. 4. The output waveform of the designed VCO with and without current source.

$$I_{bias} = \frac{P_{DC}}{V_{Supply}} \tag{1}$$

where P_{DC} is the expected power consumption for the desired VCO and V_{Supply} is the supply voltage of the VCO.

In the next step, the values of the inductor parameters such as quality factor (Q) and inductance (L) must be obtained using the computer simulation. As inductors have parasitic resistances which can increase the phase noise of the VCO, in the reported design method the parasitic resistors have been taken into account. It can be shown that the parasitic resistance of an inductor in the forms of parallel and series resistors can be simply calculated as below [12]:

$$R_P = \omega_0 LQ \tag{2}$$

$$R_S = \frac{L\omega_0}{Q} \tag{3}$$

where L stands for the inductance of the inductor, ω_0 is desired operating angular frequency, Q is the highest quality factor of the inductor which is achieved by using computer simulations and R_P or R_S stands for the parallel or series parasitic resistor of the inductor respectively.

Moreover, in Fig. 3, the output voltage (V_{OUT}) of the VCO can be calculated using Eq. (4):

$$V_{OUT} = \frac{4}{\pi} R_P I_{bias} \tag{4}$$

Next, by using the Eq. (5), main capacitor (C) will be calculated in such a way that the LC resonator to resonate in the desired operating angular frequency of the ω_0 as:

$$\omega_0 = \frac{1}{\sqrt{LC}}\sqrt{1-\frac{R_S^2 C}{L}} \tag{5}$$

So, using the design method which is based on the fundamental equations, the required values for inductors, capacitor and the current source have been calculated. As we have mentioned earlier, in this paper we have used Class-B LC VCO core model to develop our design method. As our goal is to design a LC VCO in CMOS technology, the implemented active components are MOSFETs. Therefore, it is required to calculate the size of the MOSFETs in order to improve the VCO performance in the expected operating frequency. For this reason, the oscillation condition is first defined in Eq. (6):

$$g_m \geq \alpha \frac{R_S C}{L} \tag{6}$$

where R_S the parasitic series resistance of the inductor, C and L are the capacitance and inductance of the VCO respectively which have been already calculated by Eq. (3) and Eq. (5). Also, Eq. (6) estimates the resonator loss and suggests the minimum conductivity (g_m) in order to compensate this loss using MOSFETs. Moreover, in Eq. (6), α is the loop gain of the oscillator as shown in Fig.1. As described in [8] the value of α should be greater than 1 (α >1).

In the next step, the widths of the MOSFETs are calculated having g_m from Eq. (6) and using the following equation [13]:

$$W = \frac{g_m L_c}{k_n (V_{gs} - V_t)} \tag{7}$$

In Eq. (7), L_c is the channel length of the MOSFET which depends on the technology implemented for the design of the VCO, k_n is the transcondanctance of the NMOS, V_{gs} is the gate-source voltage used for biasing the transistor and V_t is the MOSFET threshold voltage. Generally, V_{gs} should be selected in such a way that $V_{gs} - V_t$ is neither too small nor too large. Although small values of $V_{gs} - V_t$ reduces the power consumption, it increases the transistor width which will oversize the VCO. However, large values of $V_{gs} - V_t$ will deteriorate g_m which in turn increases the power consumption [14]. Thus, it is important to select a reasonable value for $V_{gs} - V_t$ which in this paper, it has been chosen to be 0.5V after simulation of the utilized MOSFETs in the VCO core

Then, the related varactor parameters must be extracted by simulation in order to have a specific tuning range. To perform the simulation, all our expected tuning range (minimum and maximum frequencies) is firstly defined. Secondly, the minimum and maximum values of the main capacitor related to the maximum and minimum frequencies must be calculated using the value of the inductor which is fixed in the whole frequency range. These two steps can be done using the Eq. (5). Now the desired varactor parameter should have this capability to cover the capacitor range which has been calculated from minimum and maximum frequencies.

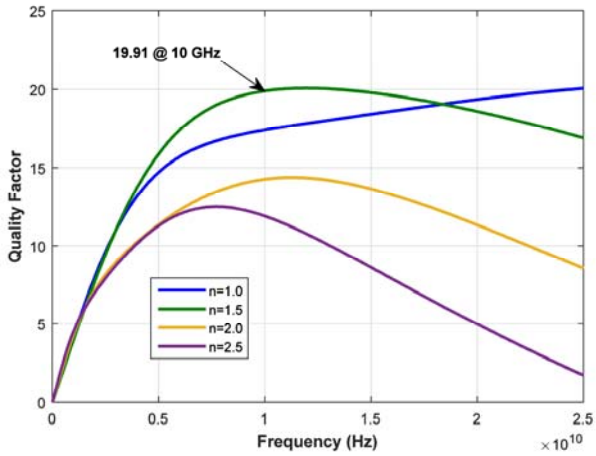
As the varactor has been used in the VCO, the phase noise characteristic will be degraded by few decibels due to this fact that the varactor will import more parasitic capacitances into the circuit which in turn deteriorates the phase noise.

It is important to note that after adding the varactor to the VCO, the total value of the capacitance in the circuit will increase and therefore according to Eq. (5), the operating frequency will decrease. Thus for avoiding the shift in the frequency from the desired operating frequency we need to decrease the main capacitor value (C), to keep the VCO working in the center frequency of the ω_0.

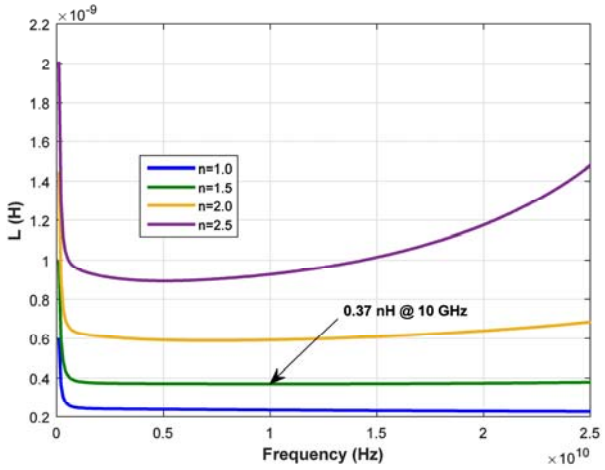
III. Results and Discussions

In this paper, a new VCO based on the reported design method will be presented which operates in X frequency band. The architecture of our designed VCO is the conventional one, however further optimization has been applied to the circuit components using the proposed algorithm in Fig.2 in order to boost up the VCO performance. In our design method we will first assign a pre-determined power consumption value which is 1.8 mw. Then the operating frequency is set at 10 GHz which is center frequency in the X frequency band. Next, using Eq. (1), the bias current for the current source is calculated to be 1 mA because the supply voltage of the VCO core is 1.8 V. In the next part, the inductor parameters have been extracted using KeySight ADS software.

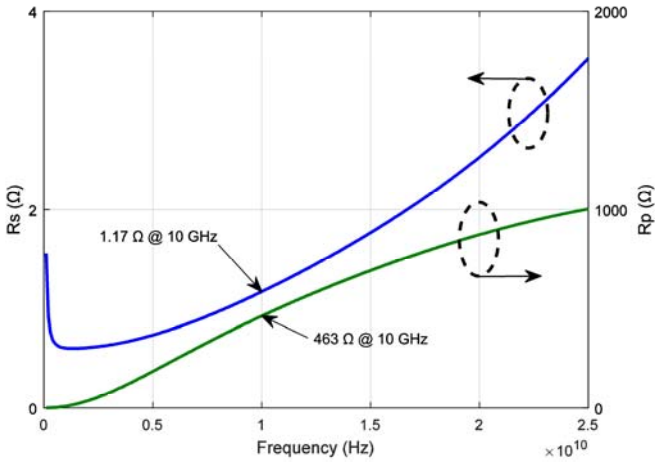
Fig. 5 shows our proposed inductor characteristics. Using Fig. 5(b), the inductance value can be simply determined in the working frequency of 10 GHz. Using Eq. (5), the main capacitor value C, in the VCO core circuit will be calculated. From the values of the parasitic series and parallel resistances which are determined from Fig. 5(c), the minimum g_m that is required to start the oscillation can be calculated. In other words, the negative resistance that is necessary for the compensation of the resonator loss is calculated using Eq. (6.). The MOSFETs widths are then calculated from the obtained g_m using Eq. (7). As the desired tuning range of our designed VCO is 1GHz, therefore the expected minimum and maximum frequencies of the proposed VCO are 9.5 GHz and 10.5 GHz respectively. The required minimum and maximum main capacitors have been calculated using Eq. (5). In this paper, accumulation mode of MOS structure has been used for designing the varactor, which its characteristic is shown in Fig. 6 and almost covers the capacitance



(a)



(b)



(c)

Fig. 5. Inductor parameters used in the proposed designed VCO (a) Quality factor swept across several frequencies based on number of turns (n) of the inductor (b) Inductance value in different frequencies based on number of turns (n) of the inductor (c) R_P and R_S characteristics as parasitic parallel and series resistance of the designed inductor.

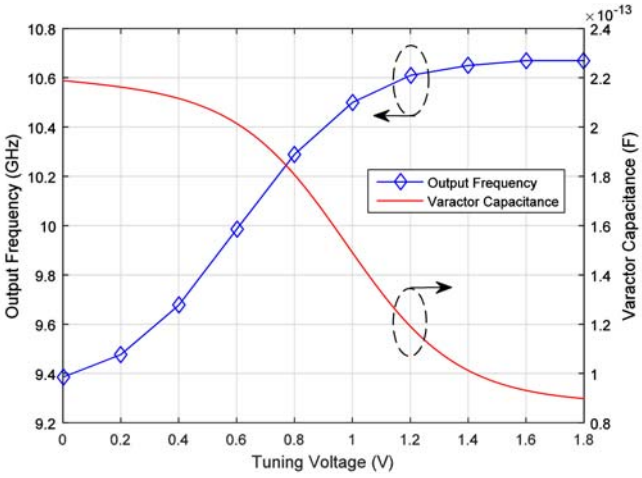


Fig. 6. The final VCO frequency coverage together with the varactor capacitance.

range (Cmax -Cmin), ensuring coverage of the defined frequency range in the proposed VCO. It should be mentioned that after adding the varactor to the VCO circuit, the main capacitor value, (C), has been decreased to prevent the shift in the operating frequency.

As can be seen in Fig. 6, not only the tuning range of the designed VCO can cover the desired frequency range which was 9.5 GHz to 10.5 GHz, but also after simulation, the tuning range is a little wider than the desired frequency and can cover the frequencies from 9.39 GHz to 10.67 GHz using tuning voltages of 0 to 1.8 V. Moreover, the characteristic of the utilized accumulation mode MOS varactor in the designed VCO is very smooth and because it has a wide transition from maximum to minimum capacitance, therefore it will result in a smooth frequency variation in the VCO output.

In order to validate the phase noise performance, the circuit has been simulated in both Cadence Spectre and KeySight ADS in which the obtained characteristics are shown in Fig. 7. Since the same 180 nm technology files have been used for the simulation purposes, the characteristics in Fig. 7 are very close to each other. The best value for the simulated phase noise of the designed VCO in KeySight ADS in its highest tuning voltage is -110.94 dBc/Hz at 1 MHz offset frequency from the carrier signal at 10.67 GHz.

As shown in Fig. 8, the amount of phase noise in the designed VCO is not constant across the whole tuning range which means at different tuning voltages the phase noise will be different and this behavior is related to the varactor in the VCO.

In VCOs, due to the relation of different performance parameters with each other, it is very challenging to evaluate the overall performance of the designed VCOs. As an example, power consumption and phase noise are inversely related to each other according to the Leeson's equation as below [15]:

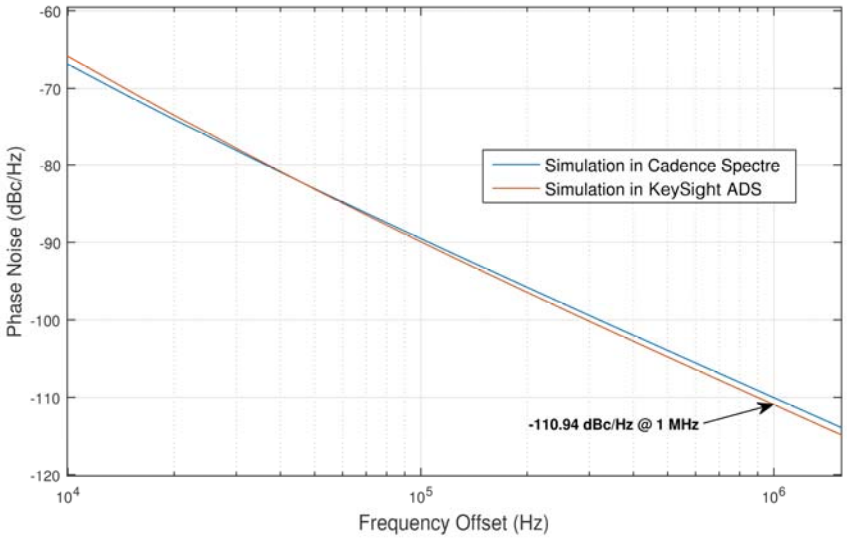


Fig. 7. Simulated phase noise of the proposed VCO in two different simulation engines while the tuning voltage has been set on 1.8 V.

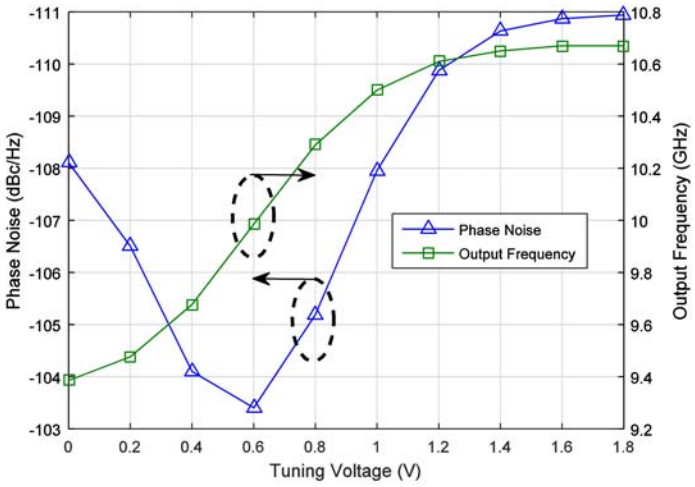


Fig. 8. Phase noise variations in different tuning voltages together with output frequency variations.

$$L(\Delta\omega) = 10\log\left\{\frac{2FKT}{P_{AV}}\left[1+\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right].\left[1+\frac{\omega_{1/f^3}}{\Delta\omega}\right]\right\} \quad (8)$$

where F is the noise factor, K is the Boltzmann's constant, T is the temperature, P_{AV} is the average power consumption of the resonator circuit, Q_L is the loaded quality factor of the resonator, ω_0 is the operating frequency of the VCO, $\Delta\omega$ is the offset frequency, ω_{1/f^3} is the corner frequency and $L(\Delta\omega)$ is the phase noise. Hence, in VCO design, there is one index which is referred to as Figure of Merit (FOM) that can cover key performance parameters of the circuit which are phase noise, power

Table I. Performance comparison of the proposed VCO.

Technology	**BW (MHz)**	**f_0 (GHz)**	**PN @ 1 MHz offset (dBc/Hz)**	**FOM (dBc/Hz)**	**FOM_T (dBc/Hz)**	**Power consumption (mW)**	**[Ref]**
65 nm CMOS	3100	7.9	-105	-178.2	-190.1	3	[18]
65 nm CMOS	1020	11.17	-107.7	-185.2	-184.4	2.2	[19]
0.18 um CMOS	3050	12.7	-104.5	-182.8	-190.4	2.4	[20]
0.13 um CMOS	870	10	-105.9	-181	-179.8	3.07	[21]
65 nm CMOS	6200	10	-104	-170.6	-186.4	22	[22]
90 nm CMOS	42	9.96	-100	-171.5	-144	7.1	[23]
0.18 um CMOS	55	7.9	-108.3	-179.3	-156.2	4.9	[24]
0.18 um CMOS	1450	10	-102	-166.4	-169.6	36	[25]
0.18 um CMOS	**1280**	**10.67**	**-110.94**	**-188.95**	**-190.5**	**1.8**	**This Work**

consumption and operating frequency [12]. By calculation of FOM for a VCO, one can compare the performances of various VCOs. FOM is defined by Eq. (9) and has been calculated to be -188.95 dBc/Hz for our proposed VCO when its power consumption is 1.8 mW and operates at 10.67 GHz at offset frequency of 1 MHz

$$FOM = L(\Delta\omega) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right) \tag{9}$$

In Eq. (9), $L(\Delta\omega)$ is the phase noise of the VCO in the operating frequency of f_0 and offset frequency of Δf and P_{diss} is the total dissipated power of the VCO in the operating frequency of f_0. Additionally, the proposed VCO has Figure of Merit including Tuning range (FOM_T) of -190.5 dBc/Hz which has been estimated using Eq. (10) [16].

$$FOM_T = FOM - 20\log\left(\frac{FTR}{10\%}\right) \tag{10}$$

where FTR stands for the Frequency Tuning Range and is obtained from difference of the upper and the lower limits of the VCO frequencies divided by the oscillation frequency [17]. Table I compares the performance of our designed VCO with those of the state-of-the-art designs.

IV. CONCLUSIONS

In this research paper, a systematic design method using negative resistance technique to reduce the phase noise and the power consumption has been presented. The method applied to a Class-B VCO in 0.18 um CMOS technology, and the maximum Figure of Merit (FOM) of -188.95 dBc/Hz was obtained. The simulated phase noise is -110.94 dBc/Hz at 1 MHz offset frequency while the dissipating power is 1.8 mW and the maximum output power of the VCO signal is 6.24 dBm.

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